**THE CLAIMS**

Kindly amend the claims as follows:

1. (currently amended) An arrangement for reducing non-linearity within an active resistor network, comprising:

a first active device adapted to provide resistance of a desired resistor, said first active device having a non-linear response, said first active device being coupled to receive a first control signal for regulating the resistance of said arrangement; and

a second active device coupled to said first active device, said second active device having a non-linear response adapted to compensate substantially for said non-linear response of said first active device, said second active device being coupled to receive a second control signal for regulating the resistance of said arrangement.

2-3. (canceled)

4. (currently amended) The arrangement of claim ~~3~~ 1 wherein one of said first and second active devices is a p-type device and the other of said first and second active devices is an n-type device.

5. (original) The arrangement of claim 4 wherein said first and said second active devices are CMOS devices.

6. (original) The arrangement of claim 5 wherein said first and said second active devices are provided with minimum dimensions for optimal high frequency performance.

7. (original) The arrangement of claim 6 wherein said first and said second active devices are tuned using an optimisation algorithm.

8. (original) The arrangement of claim 6 wherein said first and said second active devices are tuned using a manual tuning technique.

9. (currently amended) An active resistor network comprising an arrangement, said arrangement comprising a first active device adapted to provide resistance of a desired resistor, said first active device having a non-linear response, said first active device being coupled to receive a first control signal for regulating the resistance of said arrangement; and a second active device coupled to said first active device, said second active device having a non-linear response adapted to compensate substantially for said non-linear response of said first active device, said second active device being coupled to receive a second control signal for regulating the resistance of said arrangement.

10-11. (canceled)

12. (currently amended) The network of claim ~~11~~ 9 wherein one of said first and said second active devices is a p-type device and the other of said first and said second active devices is an n-type device.

13. (original) The network of claim 12 wherein said first and said second active devices are CMOS devices.

14. (original) The network of claim 13 wherein said first and said second active devices are provided with minimum dimensions for optimal high frequency performance.

15. (original) The network of claim 14 wherein said first and said second active devices are tuned using an optimisation algorithm.

16. (original) The network of claim 14 wherein said first and said second active devices are tuned using a manual tuning technique.

17. (currently amended) A method for reducing non-linearity within an active resistor network, comprising:

providing a first active device adapted to provide resistance of a desired resistor, the first active device having a non-linear response, said first active device being coupled to receive a first control signal for regulating the resistance of said arrangement; and

providing a second active device coupled to the first active device, the second active device having a non-linear response adapted to compensate substantially for the non-linear response of the first active device, said second active device being coupled to receive a second control signal for regulating the resistance of said arrangement.

18-19. (canceled)

20. (currently amended) The method of claim ~~19~~ 17 wherein one of said first and said second active devices is a p-type device and the other of said first and said second active devices is an n-type device.

21. (original) The method of claim 20 wherein said first and said second active devices are CMOS devices.

22. (original) The method of claim 21 wherein said first and said second active devices are provided with minimum dimensions for optimal high frequency performance.

23. (original) The method of claim 22 wherein said first and said second active devices are tuned using an optimisation algorithm.

24. (original) The method of claim 22 wherein said first and said second active devices are tuned using a manual tuning technique.